Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A processing core for executing instructions, comprising:

a first source register including a plurality of source fields;

a second source register including a plurality of result field select values and a plurality of operation fields;

a multiplexer coupled to at least one of the source fields;

a destination register including a plurality of result fields; and

an operand processor coupled to at least one of the result fields, wherein the operand processor and multiplexer operate upon at least one of the plurality of source fields.

2. (Original) The processing core of claim 1, wherein:

the multiplexer includes a mux input, a select input and a mux output; and

the operand processor includes a processor input, a processor output and a condition input.

3. (Original) The processing core for executing instructions of claim 2, wherein the mux input is coupled to at least one of the source fields.

4. (Original) The processing core for executing instructions of claim 2, wherein the select input is coupled to at least one of the result field select values.

5. (Original) The processing core for executing instructions of claim 2, wherein the processor input is coupled to the mux output.

6. (Original) The processing core for executing instructions of claim 2, wherein the condition input is coupled to at least one of the operation fields.

7. (Original) The processing core for executing instructions of claim 2, wherein the processor output is coupled to at least one of the result fields.

8. (Original) The processing core for executing instructions of claim 1, wherein the operand processor performs an operation selected from a group consisting of:

setting each bit from the source field low,

extension of a highest order bit of the source field to remaining bits,

bitwise inversion of the source field,

setting each bit of the source field high,

inversion of the highest order bit of the source field and extension of the highest order bit to remaining bits,

bitwise reversion of the source field,

extension of the lowest order bit of the source field to remaining bits,

bitwise inversion and reversion of the source field, and

inversion of the lowest order bit of the source field and extension of the inverted highest order bit to remaining bits.

9. (Original) The processing core for executing instructions of claim 1, wherein the operand processor selectively stores a result in one of the result fields.

10. (Original) A method for performing an operation in a data processing machine, the method comprising steps of:

selecting a source field from a source register having a first bit numbering;

manipulating the first source field to produce a result different from the source field; and

storing the result in a result field of a destination register having a second bit numbering, wherein:

the first and second bit numberings are identical,

the result originates from the source field having a first range included in the first bit numbering,

the result field has a second range included in the second bit numbering,

the first range is different from the second range; and

the manipulating and storing steps are associated with the same instruction issue.

11. (Original) The method for performing the operation in the data processing machine as recited in claim 10, further comprising a step of loading the source field from the source register.

12. (Original) The method for performing the operation in the data processing machine as recited in claim 10, wherein the manipulating step includes a step selected from a group consisting of:

setting each bit from the source field low,

extending a highest order bit of the source field to remaining bits,

bitwise inverting the source field,

setting each bit of the source field high,

inverting the highest order bit of the source field and extending the highest order bit to remaining bits,

bitwise reverting the source field,

extending the lowest order bit of the source field to remaining bits,

bitwise inverting and reverting of the source field, and

inverting of the lowest order bit of the source field and extending the inverted highest order bit to remaining bits.

13. (Original) The method for performing the operation in the data processing machine as recited in claim 10, wherein the source field is eight bits wide.

14. (Currently Amended) A method for performing an operation in a data processing machine, the method comprising steps of:

loading a first source field from a source register;

loading a second source field from the source register;

manipulating the first source field to produce a first result;

manipulating the second source field to produce a second result;

storing the first result in a second result field of a destination field; and

storing the second result in a first result field of the destination field, wherein at least three of the preceding steps are associated with a single **instruction** ~~issue~~.

15. (Original) The method for performing the operation in the data processing machine of claim 14, wherein the result field is eight bits wide.

16. (Original) The method for performing the operation in the data processing machine of claim 14, wherein the first result is different from the first source field.

17. (Original) The method for performing the operation in the data processing machine of claim 14, wherein the second result is different from the second source field.

18. (Original) The method for performing the operation in the data processing machine of claim 14, wherein the manipulation step includes a step selected from a group consisting of:

setting each bit from the source field low,

extending a highest order bit of the source field to remaining bits,

bitwise inverting the source field,

setting each bit of the source field high,

inverting the highest order bit of the source field and extending the highest order bit to remaining bits,

bitwise reverting the source field,

extending the lowest order bit of the source field to remaining bits,

bitwise inverting and reverting of the source field, and

inverting of the lowest order bit of the source field and extending the inverted highest order bit to remaining bits.

19. (Original) The method for performing the operation in the data processing machine of claim 14, wherein the loading, storing and manipulating steps are part of a same instruction issue.

20. (New) The method for performing the operation in the data processing machine of claim 14, wherein the single instruction is a sub-instruction part of a VLIW instruction word.

21. (New) The method for performing the operation in the data processing machine of claim 14, wherein all of the steps are associated with a single instruction.